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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,946	10/22/2003	John D. Anderson	A-8764	6186

5642 7590 02/21/2007

SCIENTIFIC-ATLANTA, INC.
INTELLECTUAL PROPERTY DEPARTMENT
5030 SUGARLOAF PARKWAY
LAWRENCEVILLE, GA 30044

EXAMINER	
CAVALLARI, DANIEL J	
ART UNIT	PAPER NUMBER
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	02/21/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 02/21/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTOmail@sciatl.com

Office Action Summary	Application No.	Applicant(s)	
	10/690,946	ANDERSON ET AL.	
	Examiner	Art Unit	
	Daniel J. Cavallari	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,18,21 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21, 27-30* is/are allowed.

6)☒ Claim(s) *1-3,5-11,18 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges a submission of the amendment filed on 10/24/2007. The amendments to claims 1-3, 5, 6, 10-11, 18, 21, cancellation of claims 4, 12-17, 19-20 & 22 and new claims 23-30 are accepted.

The previously made 112 rejection of claims 4 & 18 has been withdrawn. The examiner notes that the use of the term "inverting switch" will be taken to mean any device capable of performing any form of electrical inversion and is not limited to either a conventional switch nor a conventional inverter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 & 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Eitan et al. (US 5,886,561).

Eitan et al. teaches:

In regard to Claims 1

- A threshold detector circuit, read on by comparator (20).

- A first switching circuit (24) for enabling access to a back-up power source (14), the first switching circuit comprising at least one transistor (24).
- An inverting switch (22) coupled between the first switching circuit (24) and the threshold detector circuit (20), the inverting switch comprising an input and an output, the inverting switch configured to receive a signal at the input, invert the signal, and provide the inverted signal at the output, the inverting switch further configured to provide a switching delay during on-to-off transition at the output [The examiner notes the inverter inverts the input (point 21) and provides it to the output (gate of transistor 26) and further notes that all physical semiconductor components are not ideal or instantaneous and incorporate a delay between the input and output].
- Wherein the threshold detector circuit (20) is configured to cause the first switching circuit (24) to enable access to the back-up power source (14) responsive to the voltage provided by a primary power source dropping below a predetermined threshold (See Column 3, Lines 1-15).

(See Figure 1)

In regard to Claim 2

- A second switching circuit, read on by transistor switch (26) enabling access to a primary source.

In regard to Claim 3

- The threshold detector (20) is configured to cause the first switching circuit to enable or terminate access to the main power source responsive to the voltage provided by a primary power source rising above a predetermined threshold (See Column 3, Lines 35-63 & Column 1, Line 62 to Column 2, Line 11).

In regard to Claim 5

- Wherein the inverting switch (22) comprises at least one transistor [The examiner notes that Eitan discloses an inverter (53) comprising transistors (See Figure 4)].

Claims 1, 6-11, 18, & 23-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Little et al. (US 4,908,790).

In regard to Claim 1

- A threshold detector circuit, read on by comparator (32).
- A first switching circuit (14) for enabling access to a back-up power source (19), the first switching circuit comprising at least one transistor (14).
- An inverting switch (63) coupled between the first switching circuit (14) and the threshold detector circuit (32), the inverting switch comprising an input and an output, the inverting switch configured to receive a signal at the input, invert the signal, and provide the inverted signal at the output, the inverting switch further configured to provide a switching delay during on-to-off transition at the output

[The examiner notes the inverter inverts the input (from inverter 62) and provides it to the output (gate of transistor 18) and further notes that all physical semiconductor components are not ideal or instantaneous and incorporate a delay between the input and output].

- Wherein the threshold detector circuit (32) is configured to cause the first switching circuit (14) to enable access to the back-up power source (19) responsive to the voltage provided by a primary power source (11) dropping below a predetermined threshold (See Column 5, Lines 41-62 & Column 7, Line 55 to Column 8, Line 5).

[The examiner notes that the first switch (14) enables access to the back-up power supply by disconnecting power to a primary power supply (11)].

In regard to Claim 6

- An inverter (62, 34) coupled between the inverting switch (63) and the threshold detector circuit (32) (See figure 1).

In regard to Claim 7

- The inverter (62, 34) further comprising a comparator (34) (See Figure 1).

In regard to Claim 8

- A second transistor (18) coupled to the first transistor (14) (See Figure 1).

In regard to Claim 9

- The emitter of the first transistor is coupled to the collector of the second transistor (See Figure 1).

In regard to Claim 10

- Wherein current flow between the first and second transistor terminates access to the back-up power source [The examiner notes that current flow between the first (18) and second (14) transistors (between the primary source 11 and load 17) terminates access to the back-up power source when the voltage is above the predetermined value thus supply power (and current) to the load and between the switches (See figure 1)].

In regard to Claim 11

- Wherein resistance to current flow between the first and second transistors enables access to the back-up power source [The examiner notes that resistance between the switches (14 & 18) is read on by the switches being open which enables access ot the back-up power source (19) (See figure 1)].

In regard to Claim 18

A system comprising:

- A threshold detector circuit, read on by comparator (32).

- A first switching circuit (14) for enabling access to a back-up power source (19), the first switching circuit comprising at least a first transistor.
- A second switching circuit (28) enabling access to a primary power source (11), the second switching circuit comprising at least one transistor (See Figure 1) [The examiner notes that the first and second switching circuits enabling access to the back-up and primary power sources respectively by disconnecting the back-up or primary power source, respectively thus enabling access to the other power source].
- An inverting switch (63, 34, 48) coupled between the first switching circuit and the threshold detector circuit, the inverting switch configured to provide a delayed-ff output during an off-to-on transition at an input of the inverting switch [The examiner notes that the switch is configured to provide a delay by the fact that all electrical components are not ideal and require some delay in their operation].
- An inverter (62) coupled between the inverting switch (63) and the threshold detector circuit (32) (See figure 1).
- Wherein the threshold detector circuit is configured to cause the first switching circuit (14) to enable access to the back-up power source responsive to a voltage provided by a primary power source dropping below a predetermined threshold (See Column 5, Lines 41-62 & Column 7, Line 55 to Column 8, Line 5).
- Wherein the threshold detector circuit is configured to cause the second switching circuit (28) to enable access to the primary source responsive to a

voltage provided by a primary power source rising above a predetermined threshold (See Column 5, Lines 41-62 & Column 7, Line 55 to Column 8, Line 30).

In regard to Claim 23

- The inverting switch comprises at least one transistor (48) (See figure 1).

In regard to Claim 24

- Wherein the inverter comprises a comparator (34) (See Figure 1).

In regard to Claim 25

- Wherein the first switching circuit (14) comprises a second transistor (18) coupled to the first transistor (14), an emitter of the first transistor coupled to a collector of the second transistor (See Figure 1).

In regard to Claim 26

- Wherein current flow between the first and second transistor terminates access to the back-up power source [The examiner notes that current flow between the first (18) and second (14) transistors (between the primary source 11 and load 17) terminates access to the back-up power source when the voltage is above the predetermined value thus supply power (and current) to the load and between the switches (See figure 1)].

- Wherein resistance to current flow between the first and second transistors enables access to the back-up power source [The examiner notes that resistance between the switches (14 & 18) is read on by the switches being open which enables access to the back-up power source (19) (See figure 1)].

Allowable Subject Matter

Claims 21 & 27-30 are allowed for reasons indicated in the prior office action.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Cavallari whose telephone number is (571)272-8541. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel Cavallari

February 8, 2007

CHAU N. NGUYEN
PRIMARY EXAMINER